Amendments to the Drawings:

The attached replacement drawing sheet includes changes to FIG. 3. This sheet, which includes FIG. 3, replaces the original sheet including FIG. 3. The legend "RELATED ART" has been added to FIG. 3.

Attachment: Replacement Sheet
Annotated Sheet Showing Changes

REMARKS/ARGUMENTS

Prior to this communication, claims 1 – 54 were pending in the application. In the pending Office action, the Examiner rejected claims 1 – 10, 12, 15 – 26, 28, 31 – 44, 46 and 49 – 54. In response, Applicants are amending claims 1, 2, 5, 6, 10 – 12, 15 – 20, 22 – 24, 26 – 28, 31 – 33, 35, 36, 39, 40, 42 – 45, and 49 – 54; thus leaving claims 3, 4, 7 – 9, 13, 14, 21, 25, 29, 30, 34, 37, 38, 41, and 46 – 48 unchanged. Reexamination and reconsideration in view of the amendment and remarks contained herein are respectfully requested.

1. Drawings

The Office states that FIG. 1 includes reference characters (23, 24, 26, and 28) that are not mentioned in the description. In the specification, paragraph [0019] has been amended to include descriptions with respect to the reference characters 23, 24, 26, and 28.

The Office also states that FIG. 3 should be designated by a legend such as "RELATED ART." FIG. 3 has been amended and a legend "RELATED ART" has been added. Applicants respectfully request that the drawing objection be withdrawn.

2. Objected Claims

The Office objected to claims 2, 3, 5, 11, 17, 20, 22 – 33, 36, 37, and 42 – 45 due to informalities.

Particularly, the Office objected to claims 2, 5, 11, 17, 36, 39, 44, and 45 in reciting "the memory element" while plural memory elements were previously recited. These claims have been amended to include either "at least one of the memory elements" or "each of the memory elements." Applicants respectfully request that the objection to claims 2, 5, 11, 17, 36, 39, 44, and 45 be withdrawn.

The Office has also objected to claims 13, 14, 47, and 48 in reciting "the pnp devices" while "one pnp device" was previously recited in claims 6 and 40. Claims 6 and 40 have been amended to include "each of the bipolar devices comprises a pnp device." Applicants respectfully request that the objection to claims 13, 14, 47, and 48 be withdrawn.

The Office has also objected to claims 20, 26, and 27 in reciting "the fuse element" without antecedent basis. Claims 20, 26, and 27 are dependent from claim 19. Claim 19 has been amended to include "fuse elements." Applicants respectfully request that the objection to claims 20, 26, and 27 be withdrawn.

The Office objected to claims 22, 23, 31, and 32 in reciting "the circuit element" while plural circuit elements were previously recited. Claims 22, 23, 31, and 32 have been amended to include "bipolar elements." Applicants respectfully request that the objection to claims 22, 23, 31, and 32 be withdrawn.

Claim 23 has been amended to include "configured to isolate." Applicants respectfully request that the objection to claim 23 be withdrawn.

Claim 33 has been amended to include "memory density." Applicants respectfully request that the objection to claim 33 be withdrawn.

Claims 42 – 45 have been amended to depend from claim 41. Applicants respectfully request that the objection to claims 42 – 45 be withdrawn.

3. Claim Rejections

Claims 1, 2, 16, 35, 36, and 50 stand rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,568,783 ("Hu").

Hu discloses a recognition circuit for an ink jet printer that has a plurality of heating cells and identifying cells. Each heating cell has a heating element that is coupled with a power line, and a switch that is coupled with an address line. When voltages are applied to the power line and the address line, the switch is turned on and a current flows via the power line through the heating element. Each of the identifying cells is coupled with a corresponding power line. The recognition circuit reads an identification code from each of the identifying cells by applying voltage to corresponding power lines.

The Office asserted that a "bipolar device (one of the diodes 88) isolates a memory element (87) from another memory element (87) in the memory array." (Paragraph 3, page 5, Pending Action). The Office also asserted that the "bipolar diodes function to isolate separate

power supply lines for the separate memory elements and thus also isolate the fuses used as the memory elements." (Paragraph 3, page 5, Pending Action).

Applicants respectfully disagree. Hu teaches that:

> The electrical element 88 is a diode to control current flow direction in the identifying cell 84. When one of the power supply lines 82 is applied a voltage, the other power supply lines will not be affected because of the diode's 88 rectification function. (Col. 4, lines 20 – 24.)

In other words, Hu discloses that when a voltage is applied via the power supply line 82, for example P0 (FIG. 11 of Hu), another power supply line 82, for example P1 (FIG. 11 of Hu), is not affected. Thus, when voltage is applied to P0, only switches 73 of the power line P0 are affected, and switches 73 of the power line P2 are not affected. The diode 88 of P0 therefore controls the voltage applied to all the switches 73 of the power line P0. However, the diode 88 cannot and does not apply a voltage to a single switch 73 while isolating the other switches 73 connected to the same power line P0. Therefore, Hu does not teach or suggest "a plurality of bipolar devices, each of the bipolar devices associated with each of the memory elements and isolating the programming current in each of the memory elements from another memory element" as required in amended Claim 1.

Therefore, independent claim 1 is allowable. Dependent claims 2 – 18 also include patentable subject matter for the reasons set forth above with respect to claim 1.

Independent claim 35 requires, among other things, "isolating the programming current in each of the memory elements from another memory element in the memory array with a bipolar device." For reason discussed above with respect to claim 1, Hu does not teach or suggest "isolating the programming current in each of the memory elements from another memory element in the memory array with a bipolar device." Therefore, independent claim 35 is also allowable. As a consequence, dependent claims 36 – 52 also include patentable subject matter.

Claims 1, 2, 4, 15, 19, 21, 31, 32, 35, 36, 38, and 49 stand rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,243,109 ("Ishinaga") in view of U.S. Patent No. 4,064,493 ("Davis").

To establish a *prima facie* case of obviousness, three basic criteria must be met. *M.P.E.P.* § 706.02(j).

> First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the references or to combine the reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior[-]art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must be both found in the prior art, not in applicant's disclosure.

Id. See also In re Rougget, 149 F.3d 1350, 1355 (Fed. Cir. 1998) ("To reject claims in an application under section 103, the Examiner must show an unrebutted *prima facie* case of obviousness. In the absence of a proper *prima facie* case of obviousness, an applicant who complies with the other statutory requirements is entitled to a patent.")

Ishinaga discloses a print head with electricity-to-heat converters and a driver circuit formed on a circuit board.

Davis discloses a programmable cell for a programmable read-only memory matrix that includes a bipolar transistor having a fusible link in one of the transistor leads on the substrate. The fusible link is positioned adjacent the base-collector junction where it is heated by the junction current, causing the links to open at a low fusing current.

As amended, the subject matter of claim 1 is not obvious. Amended claim 1 requires, among other things, a programmable memory that includes a plurality of bipolar devices, and field-effect programming transistors. Each of the bipolar devices is associated with each of a plurality of memory elements and isolates the programming current in each of the memory elements from another memory element. Davis does not teach or suggest a programmable memory that includes a plurality of memory elements, "a plurality of field-effect programming transistors configured to program the memory elements with a programming current," and "a plurality of bipolar devices, each of the bipolar devices associated with each of the memory elements and isolating the programming current in each of the memory elements from another memory element in the memory array," as required by claim 1.

Amended claim 19 requires, among other things, "a plurality of field-effect programming transistors configured to program the memory elements with a programming current," and "a plurality of bipolar elements, each of the bipolar elements coupled to each of the memory elements and configured to isolate the programming current in each of the memory elements from another memory element." Davis does not teach or suggest these limitations.

Amended claim 35 requires, among other things, "programming the memory elements with a programming current with a plurality of field-effect programming transistors," and "isolating the programming current in each of the memory elements from another memory element in the memory array with a bipolar device." Like claims 1 and 19, claim 35 includes limitations related to a plurality of programming transistors to program each of the memory elements with a programming current, and a plurality of bipolar devices to isolate the programming current in each of the memory elements from another memory element. Ishinaga and Davis do not teach or suggest using a plurality of programming transistors to program each of the memory elements with a programming current, and using a plurality of bipolar devices to isolate the programming current in each of the memory elements from another memory element. Therefore, Ishinaga and Davis do not teach or suggest all the limitations in claims 1, 19, and 35.

Applicants also note that Davis teaches away from claims 1, 19, and 35. Davis discloses that "a transistor having an emitter 13, a collector 14, collector lead 15, a base 16," which is a bipolar transistor, is used to "program a desired pattern, the links to be opened are addressed in an X-Y manner by applying base drive to the proper input (Y) terminal and collector voltage to the corresponding output (X) terminal." (Col. 4, lines 11 – 17, and 43 – 47). That is, the bipolar transistor is used to program the fusible link or the memory. Therefore, Davis explicitly teaches away from using "a plurality of field-effect programming transistors configured to program the memory elements with a programming current," as required by claims 1 and 19, and as similarly set forth in claim 35. Accordingly, independent claims 1, 19, and 35 are allowable. Dependent claims 2, 4, 15, 21, 31, 32, 36, 38, and 49 are dependent from claims 1, 19, and 35, respectively. Accordingly, these claims also include patentable subject matter.

Claims 1, 2, 4 – 6, 12, 19, 21, 22, 28, 32, 35, 36, 38 – 40, and 46 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Ishinaga in view of U.S. Patent No. 4,112,505 ("Duval").

Duval discloses a programmable read only memory. The memory is arranged in a matrix that includes a plurality of memory cells arranged in rows and columns. A cell in a matrix is addressed by selecting the appropriate row and column. A destructible memory element connects a column to a row at each intersection. The currents for programming adjacent memory cells corresponding to a row of the memory are diverted by a single path.

As noted, claims 1, 19, and 35 include limitations related to using a plurality of programming transistors to program each of the memory elements with a programming current, and a plurality of bipolar devices to isolate the programming current in each of the memory elements from another memory element. Ishinaga and Duval do not teach or suggest using a plurality of programming transistors to program each of the memory elements with a programming current, and using a plurality of bipolar devices to isolate the programming current in each of the memory elements from another memory element. Therefore, Ishinaga and Duval do not teach or suggest all the limitations in claims 1, 19, and 35.

Applicants also note that Duval teaches away from claims 1, 19, and 35. Duval discloses that

> Switches 70 and 79 are closed so that fusible member F11 has the potential +V applied to it and the base of each linking transistor 85, 86 and 87 of row M5 is forward biased by being connected to ground potential via line resistances 71 to 74. In response to these voltages, currents i1, i2 and i3, respectively flow through the bases of transistors 87, 86 and 85 so that a current path is provided from column B11 through element F11 and the emitter collector paths of transistors 87, 86 and 85 to base 94 of shunt transistor 91; this current path is shunted only to connections of the bases of transistors 87, 86 and 85 to row M5. (Col. 8, lines 22 – 34.)

That is, a programming current flows through all the bases of the transistors 87, 86 and 85. Therefore, Duval explicitly teaches away from using "a plurality of field-effect programming transistors configured to program the memory elements with a programming current," and "a plurality of bipolar devices, each of the bipolar devices associated with each of the memory elements and isolating the programming current in each of the memory elements from another memory element in the memory array," as required by claims 1 and 19, and similar limitations in claim 35. Accordingly, independent claims 1, 19, and 35 are allowable. As a consequence, dependent claims 2, 4 – 6, 12, 21, 22, 28, 32, 36, 38 – 40, and 46 also include patentable subject matter.

Claims 3 and 37 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Hu in view of U.S. Patent Application No. 2004/0085405 ("Baek").

Baek discloses an ink-jet printhead that includes a substrate, an integrated circuit for driving a logic circuit to selectively drive nozzles of the printhead, and a logic circuit that controls input and output data. The printhead also includes an electrode that is used for wirings of the integrated circuit and the logic circuit and is patterned on the substrate. A plurality of heaters, which are formed on the electrode, generate heat by current applied through the electrode from the integrated circuit. A fuse array which includes a plurality of fuse members is formed on the electrode on a same plane with the heater. The printhead includes a cover member which is provided on the heater and the fuse array and in which an ink chamber and a nozzle are formed in a position corresponding to each of the heaters.

According to the Office, "it would have been obvious for a person of ordinary skill in the inkjet art at the time of the invention to use TaAl as the material for the fuses of Hu et al. as taught by Baek." (Section 7, Pending Action).

Applicants respectfully disagree.

As noted, Hu and Duval do not teach or suggest the limitations in claim 1. Furthermore, Baek does not teach or suggest "a plurality of bipolar devices, each of the bipolar devices associated with each of the memory elements and isolating the programming current in each of the memory elements from another memory element" as

required in Claim 1. That is, Hu, Duval, and Baek do not teach or suggest all the limitations in Claim 1. Therefore, Claim 3, which ultimately depends on Claim 1, includes patentable subject matter and is allowable.

Similarly, Claim 37, which ultimately depends from Claim 35, includes patentable subject matter for at least the reasons set forth with respect claim 35. Claim 37 is therefore allowable.

Claims 7, 8, 23, 24, 41, and 42 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Ishinaga in view of Duval, and further in view of U.S. Patent No. 3,697,828 ("Oakes").

Oakes discloses a semiconductor device that has an expanded guard ring overlying substantially an entire surface of a region except for an island. A relatively thin protective coating overlies the guard ring and a relatively thick protective coating overlies the island. A terminal connector contact for a wire-bonded or flip-chip device is formed on the relatively thick island portion of the protective coating. One form of this device includes a pnp transistor having an expanded p+ guard ring overlying a substantial portion of the collector surface noncontiguously surrounding the base region of the transistor. Islands of original p-type material having a relatively thick oxide coating thereon are left within the expanded p+ guard ring to support wire-bonding or flip-chip contact pads. (Abstract, Oakes).

The Office contends that "it would have been obvious to a person of ordinary skill in the inkjet art at the time of the invention to utilize p-type guards as suggested by Oakes for the pnp transistors of Ishinaga et al. in view of Duval et al." (Section 8, Pending Action).

Applicants respectfully disagree.

As remarked earlier, Ishinaga and Duval do not teach or suggest using a plurality of programming transistors to program each of the memory elements with a programming current, and using a plurality of bipolar devices to isolate the programming current in each of the memory elements from another memory element. Oakes does not teach or suggest this subject matter either. Therefore, Ishinaga, Duval, and Oakes do not teach or

suggest all the limitations in claim 1. Claims 7 and 8 ultimately depend from Claim 1 and are allowable for at least the same reasons.

Similarly, claims 23 and 24 are dependent on claim 19. Claim 19 includes patentable subject matter for at least the reasons set forth above with respect to claim 1. Therefore, claims 23 and 24 include patentable subject matter.

Claims 41 and 42 are ultimately dependent on claim 35. Claim 35 includes patentable subject matter for at least the reasons set forth above with respect to claim 1. Therefore, claims 41 and 42 include patentable subject matter.

Claims 9, 10, 25, 26, 43, and 44 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Ishinaga in view of Duval and Oakes, and further in view of U.S. Patent No. 4,723,155 ("Uchida").

Uchida discloses a fuse element formed on a field insulation film on a semiconductor substrate of n conductivity type. A first guard ring region of a second conductivity type is provided in the substrate, surrounding the semiconductor substrate region under the fuse element. A second guard ring region of a first conductivity type is formed in the substrate, surrounding the first guard ring region. Potentials are applied to the first and second guard ring regions. (Abstract, Uchida).

The Office indicated that "it would have been obvious to a person of ordinary skill in the inkjet art at the time of the invention to position the fuse memory elements of Ishinaga et al. in view of Duval et al. and Oakes with a dual n-type/p-type guard ring as taught by Uchida." (Section 9, Pending Action).

Applicants respectfully disagree.

As remarked earlier, Ishinaga, Duval, and Oakes do not teach or suggest using a plurality of programming transistors to program each of the memory elements with a programming current, and using a plurality of bipolar devices to isolate the programming current in each of the memory elements from another memory element. Uchida does not teach or suggest this subject matter either. Therefore, Ishinaga, Duval, Oakes, and

Uchida do not teach or suggest all the limitations in claim 1. Claims 9 and 10 ultimately depend from Claim 1. Therefore, Claims 9 and 10 include patentable subject matter and are allowable.

Claims 25 and 26 ultimately depend on claim 19. Claim 19 includes patentable subject matter for at least the reasons set forth above with respect to claim 1. Therefore, claims 25 and 26 include patentable subject matter. Claims 43 and 44 include patentable subject matter for similar the reasons.

Claims 17, 33, 51, and 53 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Ishinaga in view of Duval, and further in view of U.S. Patent No. 5,636,172 ("Prall").

Prall discloses a configuration for a laser fuse bank. Fuses of graduated width and variable configuration are placed so as to minimize an average distance between fuses and maximize fuse density.

As remarked earlier, Ishinaga and Duval do not teach or suggest using a plurality of programming transistors to program each of the memory elements with a programming current, and using a plurality of bipolar devices to isolate the programming current in each of the memory elements from another memory element. Further, Prall does not teach or suggest this subject matter either. Therefore, Ishinaga, Duval, and Prall do not teach or suggest all the limitations as required in claim 1. Claim 17 depends from Claim 1. Therefore, it includes patentable subject matter and is allowable.

Claim 33 is dependent from claim 19. Claim 19 includes patentable subject matter for at least the reasons set forth above with respect to claim 1. Therefore, claim 33 includes patentable subject matter.

Claim 51 depends from claim 35. Claim 35 includes patentable subject matter for at least the reasons set forth above with respect to claim 1. Therefore, claim 51 includes patentable subject matter.

Furthermore, amended claim 53 requires, among other things, a programmable memory on an inkjet printhead chip that includes a "memory array having a plurality of memory elements, programming transistors configured to program the memory elements with a programming current, and bipolar transistors, each of the bipolar transistors being associated with each of the memory elements, and configured to isolate the programming current in each of the memory elements from another memory element and having a memory density comprising a sum of areas occupied by the memory elements and the programming transistors, and wherein the memory density is at least 200 bits per square millimeter." Prall does not teach or suggest this subject matter. Therefore, Ishinaga, Duval, and Prall do not teach or suggest all the limitations as required in claim 53. Claim 53 therefore includes patentable subject matter and is allowable.

Claims 18, 34, and 52 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Ishinaga in view of Duval, and further in view of Baek and U.S. Patent No. 6,733,100 ("Fujita").

As remarked earlier, Ishinaga, Duval, and Baek do not teach or suggest using a plurality of programming transistors to program each of the memory elements with a programming current, and using a plurality of bipolar devices to isolate the programming current in each of the memory elements from another memory element. Fujita does not teach or suggest this subject matter either. Therefore, Ishinaga, Duval, Baek, and Fujita do not teach or suggest all the limitations in claim 1. Claim 18 is dependent from Claim 1. Therefore, claim 18 includes patentable subject matter.

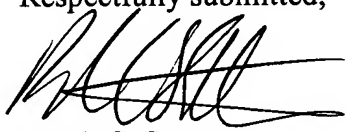
The remaining rejections of claims 34, 52, 20 and 54 fail for reasons already discussed. Therefore, these rejections should also be rescinded.

No new matter has been added.

CONCLUSION

Entry of the Amendment and allowance of claims 1 – 54 are respectfully requested. The undersigned is available for telephone consultation at any time during normal business hours.

Respectfully submitted,



Derek C. Stettner
Reg. No. 37,945

Docket No.: 059325-9036-00
Michael Best & Friedrich LLP
100 East Wisconsin Avenue
Suite 3300
Milwaukee, Wisconsin 53202-4108
414.271.6560

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Annotated Sheet Showing Changes

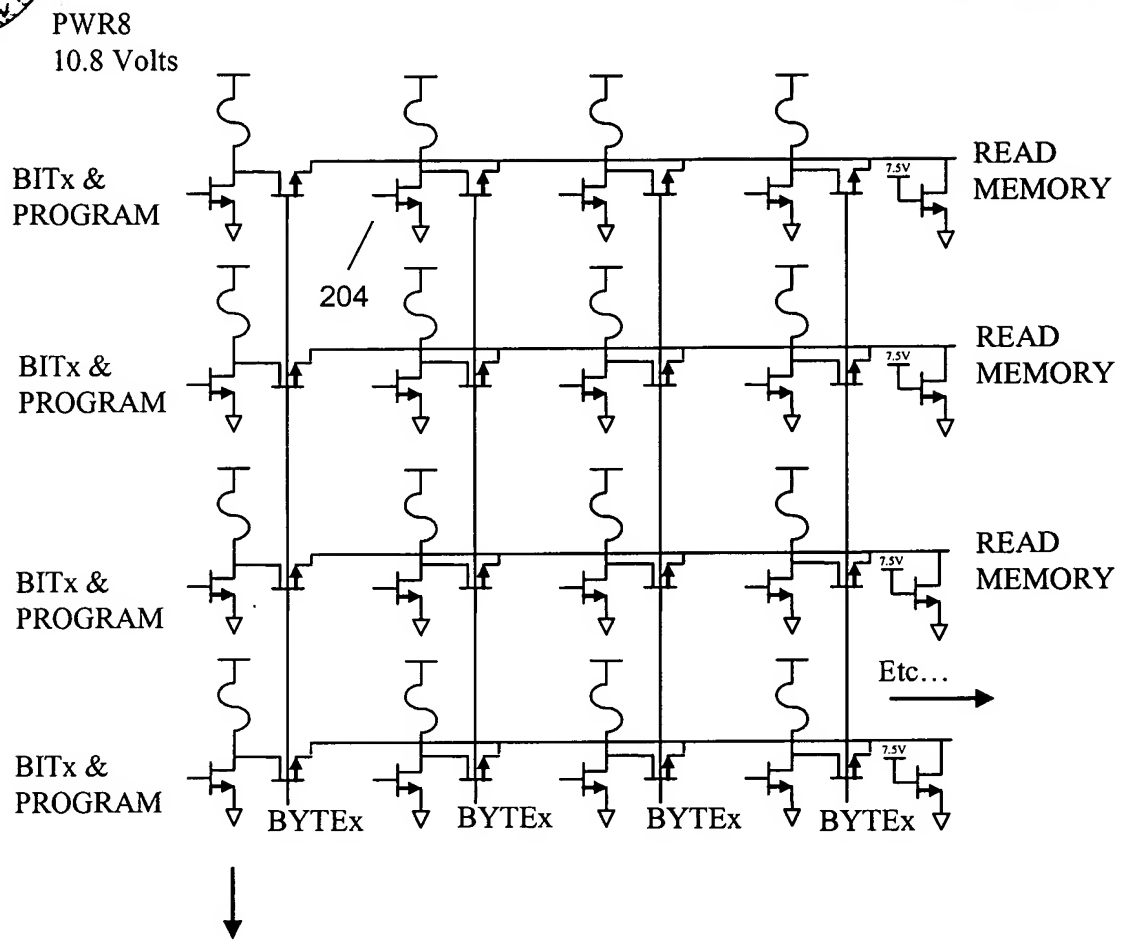

FIG. 3

RELATED ART

Label added